

5 signal pulse reshaper reshapes the phase error signal to increase the frequency of the output signal out of the lower range; and when the frequency of the output signal is in an upper range that is above the target frequency, the signal pulse reshaper reshapes the phase error signal to decrease the frequency of the output signal out of the upper range.

10 4. (original) The phase-locked loop of claim 3 wherein the lower range and the upper range are frequency ranges where the unreshaped phase error signal is incapable of synchronizing the output signal with the target frequency.

15 5. (currently amended) The phase-locked loop of claim 1 wherein the signal reshaper is a pulse reshaper and the phase error signal comprises up pulses and down pulses.

20 6. (original) The phase-locked loop of claim 5 wherein the pulse reshaper lengthens or shortens a period of a pulse of the phase error signal.

25 7. (cancelled)

8. (original) The phase-locked loop of claim 1 wherein the charge pump increases or decreases an amplitude of a current.

9. (currently amended) The phase-locked loop of claim 1 further comprising a controller that controls the signal pulse reshaper and the charge pump.

25 10. (original) The phase-locked loop of claim 1 wherein the input signal is an eight-to-fourteen modulation (EFM) signal and the output signal is a clock signal, and the phase-locked loop is incorporated into a controller of a compact disk (CD) drive or a digital versatile disk (DVD) drive.

30 11. (currently amended) A phase-locked loop of an optical disk drive controller comprising:

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14 a phase detector for receiving an eight-to-fourteen modulation (EFM) input signal and a feedback signal, and for outputting a phase error signal based on a phase difference between the input signal the feedback signal;

5 15 a charge pump connected to the phase detector for receiving the phase error signal from the phase detector and for outputting a charge pump signal, the charge pump tunable by a control signal;

10 a low pass filter connected to the charge pump for receiving the charge pump signal and outputting an clock output signal; and

15 a voltage-controlled oscillator connected between the low pass filter and the phase detector for receiving the output signal and for outputting a corresponding oscillation signal, wherein the feedback signal inputted into the phase detector is generated from the oscillation signal;

20 16 wherein according to the control signal, the charge pump is capable of outputting a charge pump signal that changes the frequency of the feedback signal to match the frequency of the input signal, and capable of outputting a charge pump signal that synchronizes the output signal with a target frequency.

25 17 12. (currently amended) The phase-locked loop of claim 11 further comprising a frequency detector connected between the voltage-controlled oscillator and the charge pump, the frequency detector for receiving the input signal and the feedback signal and for outputting a frequency difference signal to the charge pump.

30 18 13. (original) The phase-locked loop of claim 11 wherein when the frequency of the output signal is in a lower range that is lower than the target frequency, the charge pump reshapes the phase error signal to increase the frequency of the output signal out of the lower range; and when the frequency of the output signal is in an upper range that is above the target frequency, the charge pump reshapes the phase error signal to decrease the frequency of the output signal out of the upper range.

14. (original) The phase-locked loop of claim 13 wherein the lower range and the upper range are frequency ranges where the unreshaped phase error signal is incapable of synchronizing the output signal with the target frequency.

5 15. (original) The phase-locked loop of claim 11 wherein phase error signal comprises up pulses and down pulses and the charge pump as controlled by the control signal increases or decreases an amplitude of a current.

16-20. (cancelled)

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21. (new) A phase-locked loop comprising:

a phase detector for receiving an input signal and a feedback signal, and for outputting a phase error signal based on a phase difference between the input signal the feedback signal;

15 a signal reshaper connected to the phase detector for reshaping the phase error signal;

a charge pump connected to the signal reshaper for receiving the reshaped or unreshaped phase error signal from the signal reshaper and for outputting a charge pump signal, the charge pump increasing or decreasing an amplitude of a current of the charge pump signal according to the reshaped phase error signal;

20 a low pass filter connected to the charge pump for receiving the charge pump signal and outputting an output signal; and

25 a voltage-controlled oscillator connected between the low pass filter and the phase detector for receiving the output signal and for outputting a corresponding oscillation signal, wherein the feedback signal inputted into the phase detector is generated from the oscillation signal;

30 wherein the unreshaped phase error signal causes the charge pump to output a charge pump signal that changes the frequency of the feedback signal to match the frequency of the input signal, and the reshaped phase error signal causes the charge pump to output a charge pump signal that synchronizes the output signal

with a target frequency.

5 22. (new) The phase-locked loop of claim 21 further comprising a frequency detector connected between the voltage-controlled oscillator and the charge pump for receiving the input signal and the feedback signal and for outputting a frequency difference signal to the charge pump.

10 23. (new) The phase-locked loop of claim 21 wherein when the frequency of the output signal is in a lower range that is lower than the target frequency, the signal reshaper reshapes the phase error signal to increase the frequency of the output signal out of the lower range; and when the frequency of the output signal is in an upper range that is above the target frequency, the signal reshaper reshapes the phase error signal to decrease the frequency of the output signal out of the upper range.

15 24. (new) The phase-locked loop of claim 23 wherein the lower range and the upper range are frequency ranges where the unreshaped phase error signal is incapable of synchronizing the output signal with the target frequency.

20 25. (new) The phase-locked loop of claim 21 wherein the signal reshaper is a pulse reshaper and the phase error signal comprises up pulses and down pulses.

25 26. (new) The phase-locked loop of claim 25 wherein the pulse reshaper lengthens or shortens a period of a pulse of the phase error signal.

27. (new) The phase-locked loop of claim 25 wherein the pulse reshaper increases or decreases a width of a pulse.

30 28. (new) The phase-locked loop of claim 21 further comprising a controller that controls the signal reshaper and the charge pump.

29. (new) The phase-locked loop of claim 21 wherein the input signal is an

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eight-to-fourteen modulation (EFM) signal and the output signal is a clock signal, and the phase-locked loop is incorporated into a controller of a compact disk (CD) drive or a digital versatile disk (DVD) drive.

5 30. (new) A phase-locked loop comprising:

a phase detector for receiving an input signal and a feedback signal, and for outputting a phase error signal based on a phase difference between the input signal the feedback signal;

10 a signal reshaper connected to the phase detector for reshaping the phase error signal;

a charge pump connected to the signal reshaper for receiving the reshaped or unreshaped phase error signal from the signal reshaper and for outputting a charge pump signal;

15 a low pass filter connected to the charge pump for receiving the charge pump signal and outputting an output signal;

a voltage-controlled oscillator connected between the low pass filter and the phase detector for receiving the output signal and for outputting a corresponding oscillation signal, wherein the feedback signal inputted into the phase detector is generated from the oscillation signal; and

20 a controller connected to the signal reshaper and the charge pump for controlling the signal reshaper and the charge pump;

25 wherein the unreshaped phase error signal causes the charge pump to output a charge pump signal that changes the frequency of the feedback signal to match the frequency of the input signal, and the reshaped phase error signal causes the charge pump to output a charge pump signal that synchronizes the output signal with a target frequency.

31. (new) The phase-locked loop of claim 30 further comprising a frequency detector connected between the voltage-controlled oscillator and the charge pump for receiving the input signal and the feedback signal and for outputting a frequency difference signal to the charge pump.

32. (new) The phase-locked loop of claim 30 wherein when the frequency of the output signal is in a lower range that is lower than the target frequency, the signal reshaper reshapes the phase error signal to increase the frequency of the output signal out of the lower range; and when the frequency of the output signal is in an upper range that is above the target frequency, the signal reshaper reshapes the phase error signal to decrease the frequency of the output signal out of the upper range.

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10 33. (new) The phase-locked loop of claim 32 wherein the lower range and the upper range are frequency ranges where the unreshaped phase error signal is incapable of synchronizing the output signal with the target frequency.

15 34. (new) The phase-locked loop of claim 30 wherein the signal reshaper is a pulse reshaper and the phase error signal comprises up pulses and down pulses.

35. (new) The phase-locked loop of claim 34 wherein the pulse reshaper lengthens or shortens a period of a pulse of the phase error signal.

20 36. (new) The phase-locked loop of claim 34 wherein the pulse reshaper increases or decreases a width of a pulse.

37. (new) The phase-locked loop of claim 30 wherein the charge pump increases or decreases an amplitude of a current.

25 38. (new) The phase-locked loop of claim 30 wherein the input signal is an eight-to-fourteen modulation (EFM) signal and the output signal is a clock signal, and the phase-locked loop is incorporated into a controller of a compact disk (CD) drive or a digital versatile disk (DVD) drive.

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